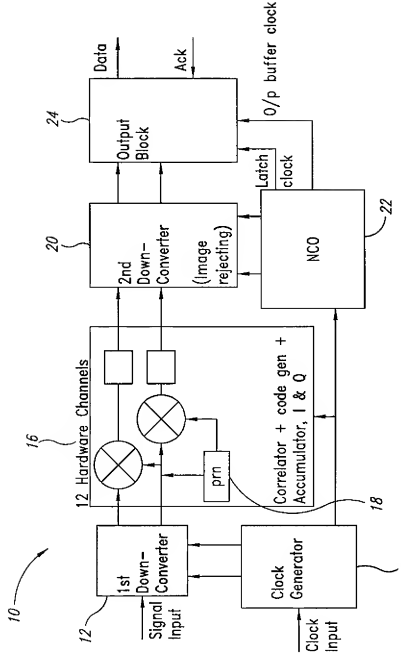
10
12
1st Down-Converter
Signal Input
Clock Generator
Clock Input
14
16
12 Hardware Channels
prn
Correlator + code gen + Accumulator, I & Q
18
20
2nd Down-Converter (Image rejecting)
22
NCO
24
Output Block
Data
Ack
O/p buffer clock
Latch clock

FIG. 2